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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/718,850	11/22/2000	Ramachandra Divakaruni	BUR9-2000-0016-US1	3171

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/718,850	DIVAKARUNI ET AL.	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. Claim 18 is objected to because of the following informalities: the word "contered" appears to be misspelled. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The scope of claim 18 is unclear because the sentence "forming in said semiconductor layer a buried collector region contered at approximately said interface". It is not clear where the location of the buried collector region is located with reference to the "interface" region. How is the interface between the buried insulator layer and the semiconductor layer defined?

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 18, in so far in compliance of 35 U.S.C. 112 is rejected under 35 U.S.C. 102(b) as being anticipated by Eklund US patent No. 5,087,580.

Regarding claim 18, Eklund teaches (figs. 2-8) a bipolar device on a SOI substrate having a buried layer insulator 10 that forms an interface with an overlying semiconductor layer 16, comprising the steps forming in the semiconductor layer a buried collector region centered at approximately the interface and forming in the semiconductor layer a base region vertically stacked on the buried collector region.

Regarding claim 19, Eklund teaches the entire process step of claim 18 above including the buried collector region and the base region are formed by implantation through a single mask formed on the SOI (figs. 2-8).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5, 7-18 and 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Eklund US patent No. 5,087,580 in view of Blair US patent No. 5,904,536.

Regarding claim 1, Eklund teaches a method (figs. 2-8) of forming an emitter in a vertical bipolar transistor comprising: providing a substrate 16 having a collector layer 26 and a base layer 48 over the collector layer; forming a patterned mask over the base

layer and filling the opening in the mask with emitter material where the emitter material contacting the substrate.

Eklund does not explicitly teach, filling the opening using damascene process and does not explicitly teach filling more than one opening.

Blair teaches (figs. 2a-2j) the use of damascene process for forming a self-aligned polysilicon emitter in the process of forming a bipolar transistor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the damascene process taught by Blair in to the process of Eklund in order to form the emitter of the bipolar transistor since damascene process eliminates the need for over etching of epitaxial silicon in the base region because the process is selective to polysilicon over epitaxial silicon.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to make more than one opening and filling the openings in the mask with emitter material since the formation integrated circuit involves the fabrication of more than one bipolar transistor.

Regarding claim 2, Eklund teaches substantially the entire process steps of claim 1 above including the substrate includes an insulator layer 10 between the bottom silicon layer and a top silicon layer 16, the method further comprising implanting a first impurity to form the collector layer 26 in a lower portion of the top silicon layer adjacent the insulator layer and implanting a second impurity to form the base layer 48 in an upper portion of the top silicon layer (figs. 2-8).

Regarding claim 5, Eklund teaches substantially the entire process step of claim 1 above including forming a protective layer 74 over the emitter and implanting additional amounts of the first impurity into and through the insulator layer to provide a collector contact diffusion region 76 (fig. 8).

Regarding claim 20, Eklund teaches substantially the entire process steps of claims 18, 1 and 3 above including forming a mask having opening 54 on the SOI substrate and depositing an emitter material contacting the SOI substrate 26 having a first impurity in the opening to form an emitter 60.

Claim 3, is rejected under 35 U.S.C. 103(a) as being unpatentable over Eklund in view of Blair in view of Miwa et al. US patent No. 5,352,624.

Regarding claim 3, Eklund teaches substantially the entire process step of claim 1 above including first impurity emitter diffusion region 61 in the base below the emitter 60.

Eklund does not teach explicitly the method of claim 2 further comprising annealing the vertical bipolar transistor to drive the first impurity into the base to create an emitter diffusion region in the base below each emitter.

Annealing the vertical transistor to drive impurities into the base to create an emitter diffusion region is a conventional process and is also taught by Miwa in the process of manufacturing a bipolar transistor structure (fig. 20I, col. 39, line 63-, col. 40, line 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the conventional annealing process the process of Eklund in order to speed the diffusion process.

Claim 4, is rejected under 35 U.S.C. 103(a) as being unpatentable over Eklund in view of Blair in view of Horie US patent No. 5,406,113.

Regarding claim 4, Eklund teaches substantially the entire process steps of claim 1 above except explicitly stating that the method of claim 2 further comprising: patterning a second mask over the bipolar region the mask including openings through to the base layer between one of the emitter and implanting additional amounts of the second impurity into the base layer through the openings.

It is conventional to form openings by patterning a masking layer and also taught Horie (Horie, figs 3a-3g) with regards to bipolar structure since such structures are readily used for forming impurity regions that are subsequently used for metallization purposes.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implant impurity in the structures taught by Horie in the process of Eklund in order to reduce contact resistance between base region and base electrode.

Regarding claims 11, 7-10, and 12-17, Eklund teaches substantially the entire process steps of claims 1-5 above including the method of simultaneously forming CMOS devices and vertical bipolar transistor on an integrated circuit chip comprising: providing a silicon a silicon over insulator substrate having a collector layer 26 and a

base layer 48 over the collector layer; forming a gate oxide layer 44 only the CMOS region of the SOI substrate, forming a polysilicon layer 46 of the CMOS region of the SOI substrate pattering a mask over the polysilicon layer and the bipolar region of the SOI substrate, the mask including openings 54 over the bipolar region; depositing an emitter material to form emitters; removing the mask; patterning the polysilicon layer to form gate conductor 62 and forming sidewall spacers 74 adjacent the emitter and the gate conductors (figs. 2-8).

Eklund does not teach depositing emitter material in the openings in a damascene process and forming more than one emitter.

Blair teaches (figs. 2a-2j) the use of damascene process for forming a self-aligned polysilicon emitter in the process of forming a bipolar transistor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the damascene process taught by Blair in to the process of Eklund in order to form the emitter of the bipolar transistor since damascene process eliminates the need for over etching of epitaxial silicon in the base region because the process is selective to polysilicon over epitaxial silicon.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to make more than one opening and filling the openings in the mask with emitter material since the formation integrated circuit involves the fabrication of more than one bipolar transistor.

Response to Arguments

6. Applicant's arguments with respect to claims 1-5 and 7-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 305-7646. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tom Thomas

Samuel Admassu Gebremariam
August 20, 2002

TOM THOMAS
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